IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A semiconductor device for use in a stacked multi-chip assembly, comprising:

a semiconductor die; and

a dielectric spacer layer formed on and secured to at least a portion of a surface of the semiconductor die and protruding from the surface to space the semiconductor die substantially a predetermined distance from an adjacent semiconductor die to accommodate a height of at least one intermediate conductive element between the semiconductor die and the adjacent semiconductor die, the dielectric spacer layer protruding from the surface substantially the predetermined distance before ~~that~~ the semiconductor die ~~and an~~ is positioned adjacent to the adjacent semiconductor ~~die of the stacked multi-chip assembly are to be spaced apart from one another~~, the spacer layer including voids communicating with a lateral periphery thereof.

2. (Previously presented) The semiconductor device of claim 1, wherein the dielectric spacer layer comprises a plurality of laterally discrete spacers.

3. (Previously presented) The semiconductor device of claim 1, further comprising: at least one discrete conductive element protruding above a surface of the semiconductor die.

4. (Previously presented) The semiconductor device of claim 3, wherein the at least one discrete conductive element comprises one of a bond wire, a thermocompression bonded lead, and a tape-automated bond element.

5. (Previously presented) The semiconductor device of claim 1, wherein the predetermined distance exceeds a distance a discrete conductive element protrudes above a surface of at least one of the semiconductor die and the adjacent semiconductor die.

6. (Previously presented) The semiconductor device of claim 1, wherein the predetermined distance is about the same as or less than a distance a discrete conductive element protrudes above a surface of at least one of the semiconductor die and the adjacent semiconductor die.

7. (Previously presented) The semiconductor device of claim 1, wherein the dielectric spacer layer covers only a portion of the surface.

8. (Previously presented) The semiconductor device of claim 7, wherein the dielectric spacer layer comprises a pattern.

9. (Previously presented) The semiconductor device of claim 7, wherein the dielectric spacer layer comprises randomly arranged features.

10. (Previously presented) The semiconductor device of claim 1, wherein the dielectric spacer layer comprises a material that will adhere to a surface of the adjacent semiconductor die.

11. (Previously presented) The semiconductor device of claim 1, wherein the dielectric spacer layer comprises a polymer.

12. (Previously presented) The semiconductor device of claim 11, wherein the polymer comprises a photoimageable polymer.

13. (Previously presented) The semiconductor device of claim 1, wherein the dielectric spacer layer comprises at least one of a glass, a silicon dioxide, a silicon nitride, and a silicon oxynitride.

14. (Withdrawn) The semiconductor device of claim 1, wherein the dielectric spacer layer is positioned on an active surface of the semiconductor die.

15. (Withdrawn) The semiconductor device of claim 1, wherein the dielectric spacer layer is positioned on a back side of the semiconductor die.

16. (Withdrawn) The semiconductor device of claim 1, further comprising: another dielectric spacer layer covering at least a portion of an opposite surface of the semiconductor die.

17. (Previously presented) The semiconductor device of claim 1, further comprising: adhesive material on an exposed surface of the dielectric spacer layer.

18. (Previously presented) The semiconductor device of claim 1, wherein the dielectric spacer layer comprises a plurality of at least partially superimposed, contiguous, adhered sublayers.

19. (Currently amended) A semiconductor device assembly, comprising:

a first semiconductor device including an active surface carrying bond pads that are configured to have intermediate conductive elements secured thereto;

a nonconfluent spacer layer comprising dielectric material secured to ~~a~~ the active surface of the first semiconductor device~~;~~ and, prior to securing an intermediate conductive element to any of the bond pads, protruding from the active surface substantially a predetermined distance the active surface of the first semiconductor device is to be spaced apart from a back side of a second semiconductor device upon positioning the second semiconductor device ~~positioned~~ over the first semiconductor device so as to accommodate the

intermediate conductive elements~~, a surface of the second semiconductor device being secured to the nonconfluent spacer layer~~.

20. (Previously presented) The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises at least one void therein that communicates with a lateral periphery of the nonconfluent spacer layer.

21. (Previously presented) The semiconductor device assembly of claim 20, wherein the at least one void facilitates lateral introduction of adhesive material between the first and second semiconductor devices.

22. (Previously presented) The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

23. (Previously presented) The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer has a substantially uniform thickness.

24. (Currently amended) The semiconductor device assembly of claim 19, further comprising:

the second semiconductor device; and

at least one ~~discrete~~ intermediate conductive element protruding above the active ~~a~~ surface of ~~at least one of~~ the first ~~and second~~ semiconductor ~~devices~~ deviceand located at least partially between the first and second semiconductor devices.

25. (Currently amended) The semiconductor device assembly of claim 24, wherein the nonconfluent spacer layer has a thickness that spaces the first and second semiconductor devices apart from one another a distance that exceeds a height the at least one ~~discrete~~ intermediate conductive element protrudes above the active surface of ~~at least one of~~ the first ~~and second~~ semiconductor ~~devicesdevice~~.

26. (Currently amended) The semiconductor device assembly of claim 24, wherein the nonconfluent spacer layer has a thickness that spaces the first and second semiconductor devices apart from one another a distance that is about the same as or less than a height the at least one discrete conductive element protrudes above the active surface of ~~at least one of~~ the first ~~and second~~ semiconductor ~~devices~~device.

27. (Withdrawn) The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises dielectric material.

28. (Withdrawn) The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises a polymer.

29. (Withdrawn) The semiconductor device assembly of claim 28, wherein the polymer adheres to surfaces of the first semiconductor device and the second semiconductor device.

30. (Withdrawn) The semiconductor device assembly of claim 28, wherein the polymer comprises a photoimageable polymer.

31. (Previously presented) The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises a plurality of at least partially superimposed, contiguous, mutually adhered sublayers.

32. (Previously presented) The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

33. (Previously presented) The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises a pattern.

34. (Withdrawn) The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises randomly arranged features.

35. (Withdrawn) The semiconductor device assembly of claim 19, further comprising:
an adhesive material securing the nonconfluent spacer layer to at least one of the surface of the first semiconductor device and the surface of the second semiconductor device.

36. (Withdrawn) The semiconductor device assembly of claim 35, wherein the adhesive material is located within voids in the nonconfluent spacer layer.

37. (Currently amended) The semiconductor device assembly of claim 19, further comprising:
a substrate upon which ~~one of~~ the first semiconductor device ~~and the second semiconductor device~~ is positioned.

38. (Previously presented) The semiconductor device assembly of claim 37, wherein at least one bond pad of at least one of the first semiconductor device and the second semiconductor device is in communication with a corresponding contact area of the substrate.

39. (Previously presented) The semiconductor device assembly of claim 37, wherein the substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

40. (Canceled)

41. (Withdrawn) The semiconductor device assembly of claim 19, further comprising:
at least one additional semiconductor device.

42. (Currently amended) The semiconductor device assembly of claim 19, ~~further comprising:~~wherein the nonconfluent spacer layer comprises a plurality ~~of nonconfluent spacer~~ layers ~~between the first and second semiconductor devices~~, additive thicknesses of the plurality of ~~nonconfluent spacer~~ layers defining the substantially predetermined ~~a~~ distance ~~the first and second semiconductor devices are spaced apart from one another~~.

43. (Currently amended) The semiconductor device assembly of claim 42, wherein a first ~~nonconfluent spacer~~ layer of the plurality of ~~nonconfluent spacer~~ layers is secured to ~~a~~ the active surface of the first semiconductor device and a second ~~nonconfluent spacer~~ layer of the plurality of ~~nonconfluent spacer~~ layers is configured to be secured to ~~an opposed surface~~ the back side of the second semiconductor device.

44. (Currently amended) The semiconductor device assembly of claim 42, wherein at least some solid regions of each of the plurality of ~~nonconfluent spacer~~ layers are at least partially superimposed relative to one another.

45. (Withdrawn) A multi-chip module, comprising:
a substrate;
a first semiconductor device positioned on the substrate;
a nonconfluent layer comprising dielectric material over the first semiconductor device;
a second semiconductor device positioned over the nonconfluent layer; and
an encapsulant covering at least portions of the first semiconductor device, the nonconfluent layer, the second semiconductor device, and portions of the substrate located adjacent the first semiconductor device.

46. (Withdrawn) The multi-chip module of claim 45, wherein the substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

47. (Withdrawn) The multi-chip module of claim 45, wherein at least one bond pad of at least one of the first semiconductor device and the second semiconductor device is in electrical communication with a corresponding contact area of the substrate.

48. (Withdrawn) The multi-chip module of claim 47, wherein the electrical communication is established by at least one discrete conductive element extending at least partially between the first and second semiconductor devices and protruding above a surface of at least one of the first semiconductor device and the second semiconductor device.

49. (Withdrawn) The multi-chip module of claim 48, wherein the nonconfluent layer has a thickness that exceeds a distance the at least one discrete conductive element protrudes above the surface.

50. (Withdrawn) The multi-chip module of claim 48, wherein a thickness of the nonconfluent layer is about the same as or less than a distance the at least one discrete conductive element protrudes above the surface.

51. (Withdrawn) The multi-chip module of claim 45, wherein the nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

52. (Withdrawn) The multi-chip module of claim 45, wherein the nonconfluent layer comprises a pattern.

53. (Withdrawn) The multi-chip module of claim 45, wherein the nonconfluent layer comprises randomly arranged features.

54. (Withdrawn) The multi-chip module of claim 45, wherein the nonconfluent layer has a substantially consistent height.

55. (Withdrawn) The multi-chip module of claim 45, wherein the nonconfluent layer comprises a dielectric material.

56. (Withdrawn) The multi-chip module of claim 55, wherein the dielectric material comprises at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

57. (Withdrawn) The multi-chip module of claim 45, wherein the nonconfluent layer comprises a polymer.

58. (Withdrawn) The multi-chip module of claim 57, wherein the polymer is capable of adhering to a surface of at least one of the first semiconductor device and the second semiconductor device.

59. (Withdrawn) The multi-chip module of claim 57, wherein the polymer comprises a photoimageable polymer.

60. (Withdrawn) The multi-chip module of claim 45, wherein the nonconfluent layer comprises a plurality of at least partially superimposed, contiguous, mutually adhered layers.

61. (Withdrawn) The multi-chip module of claim 45, further comprising:
an adhesive material securing the first and second semiconductor devices to one another.

62. (Withdrawn) The multi-chip module of claim 61, wherein the adhesive material is located within voids of the nonconfluent layer.

63. (Withdrawn) The multi-chip module of claim 45, wherein the encapsulant comprises a glob-top type encapsulant.

64. (Withdrawn) The multi-chip module of claim 45, wherein the encapsulant comprises a molded encapsulant.

65. (Withdrawn) The multi-chip module of claim 45, further comprising:
a plurality of nonconfluent layers between the first and second semiconductor devices, additive thicknesses of the plurality of nonconfluent layers defining a distance the first and second semiconductor devices are spaced apart from one another.

66. (Withdrawn) The multi-chip module of claim 65, wherein a first nonconfluent layer of the plurality of nonconfluent layers is secured to a surface of the first semiconductor device and a second nonconfluent layer of the plurality of nonconfluent layers is secured to an opposed surface of the second semiconductor device.

67. (Withdrawn) The multi-chip module of claim 65, wherein at least some solid regions of each of the plurality of nonconfluent layers are at least partially superimposed relative to one another.

68-102. (canceled)